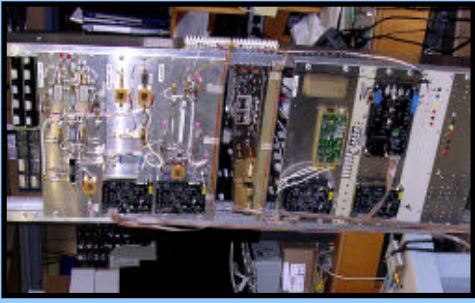



Receiver Packaging Trends

- Conventional receivers have been built in a rack mount approach costing on the order of \$100k or more
- Recent advances in packaging include the multi-module downconverter approach (DSN) and the single module downconverter approach.
- A single chip receiver is not too far in the future. A four channel 77GHz transceiver has already been designed, fabricated in SiGe, and tested by Hajimiri's group at Caltech.

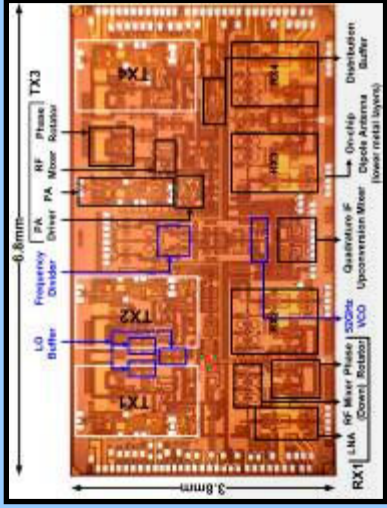
1995
EVLA
RACK
\$100k



2000 DSN Box
\$40k



2009
Receiver
on a Chip
\$10



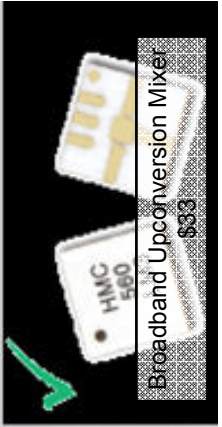
2004 Multichip
Module \$5k



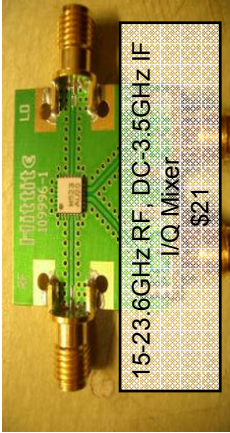
Refs: http://www.aoc.nrao.edu/evla/admin/reviews/lo-if-fo_cdr/IfSubSys_tcotter.pdf,
A. Natarajan et. al, "77 GHz Phased Array Transceiver in Silicon," presented at the Lee Workshop, 2006.

Multichip Implementation

- A block diagram of an inexpensive (~\$1500) upconversion based receiver that is being designed at Caltech appears to the right.
- New inexpensive packaged ICs (such as a 45GHz frequency doubler) make the upconversion approach affordable.
- Several of the enabling ICs appear to right.



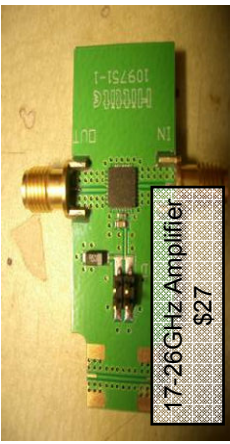
Broadband Upconversion Mixer
\$33



15-23.6GHz RF, DC-3.5GHz IF
I/Q Mixer
\$21

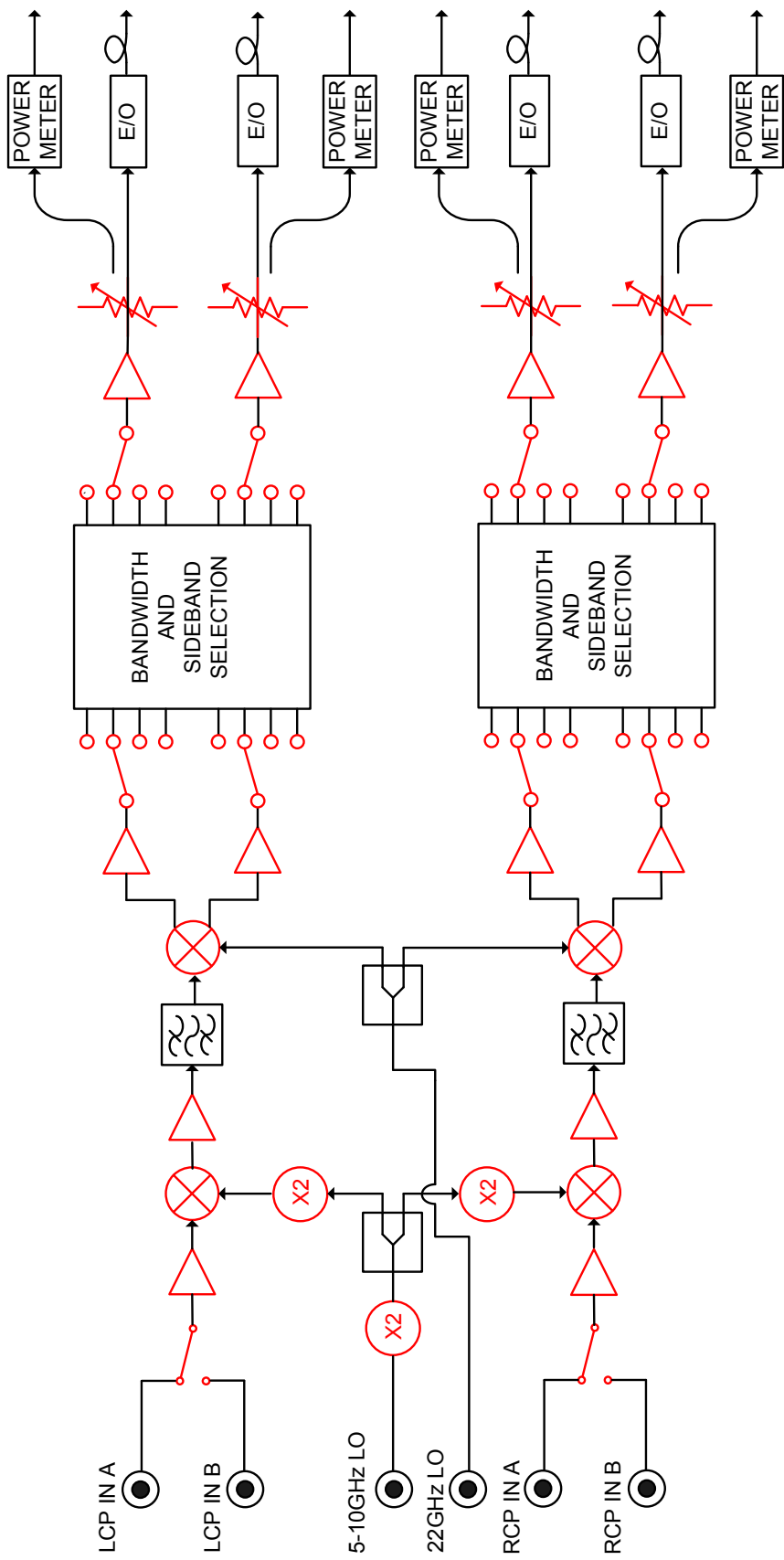


7.5-22.5/15-45GHz Active Doubler
\$28



17-26GHz Amplifier
\$27

Refs: www.hittite.com, www.mimixbroadband.com

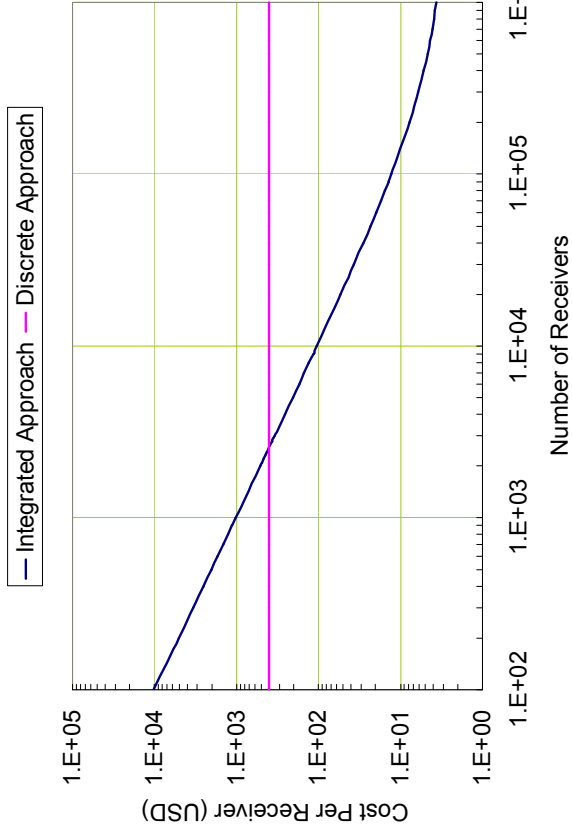


IC Cost < \$700

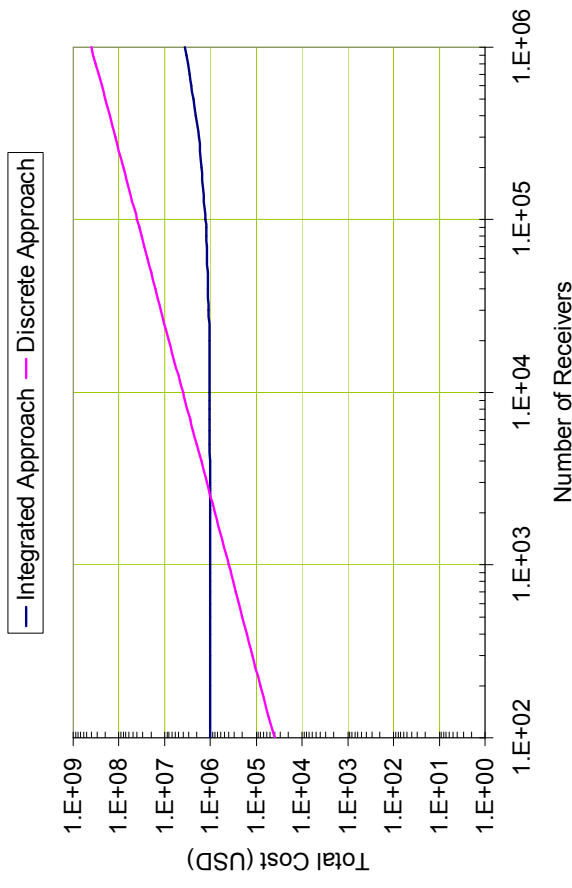
Single Chip Implementation

- Many of the components required for the upconversion approach can be replaced by a single IC. The components that can be replaced using today's SiGe processing are highlighted in red to the right.
- Economics dictates replacing these components for quantities greater than 2500.
- A Hybrid LTCC approach may allow for high Q and inexpensive offchip filtering as well as integration with photonics (see below).

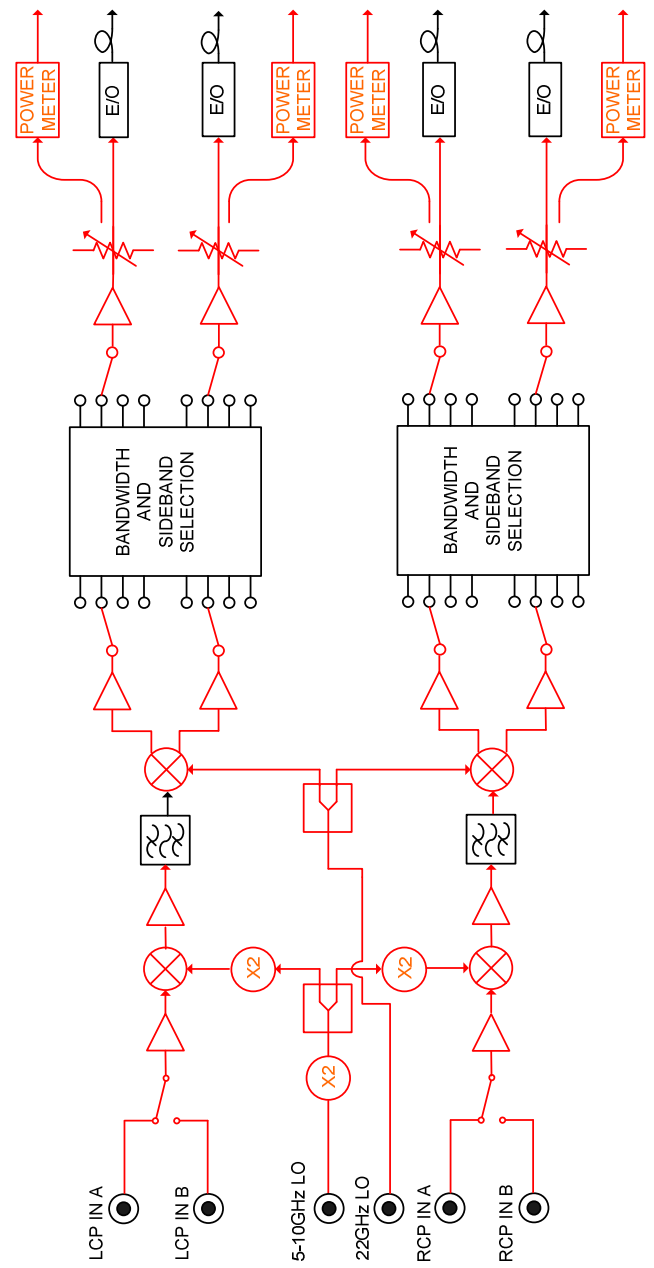
Estimated Cost Per Receiver vs Number of Receivers Needed



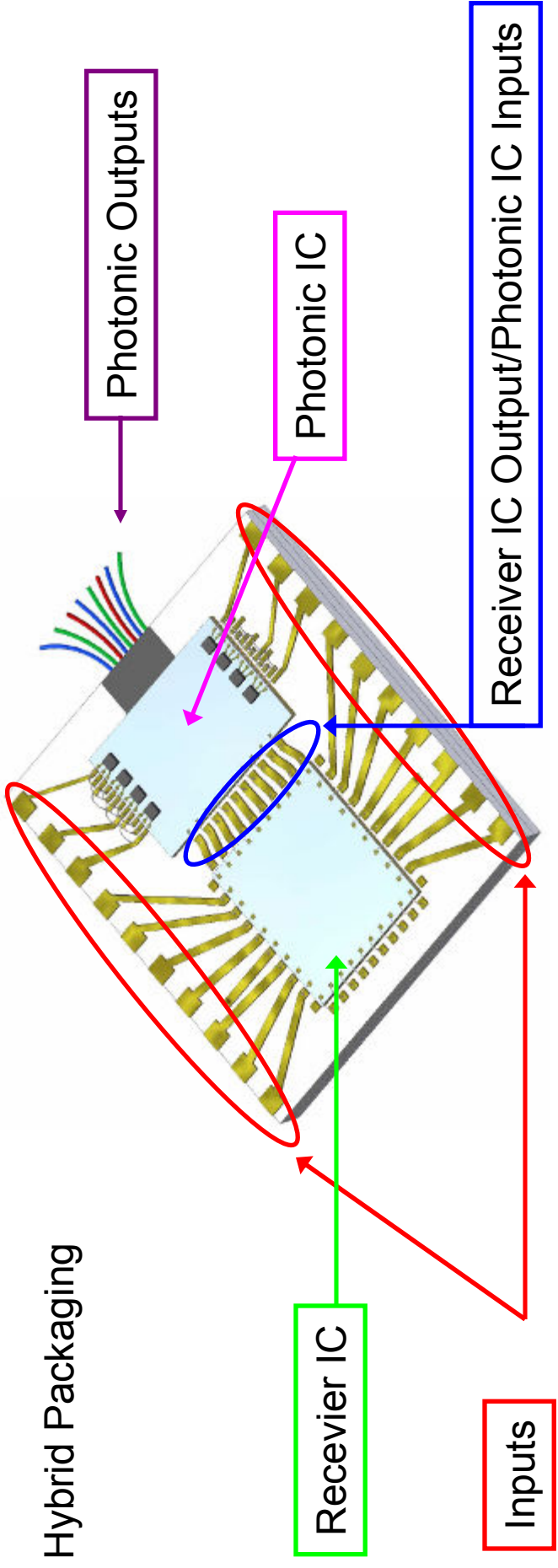
Total Cost vs Number of Receivers



Discrete approach cost includes ICs required for two channel receiver and does not include filters, bandwidth and sideband selection components, or optical components



Hybrid Packaging



CMOS photonics

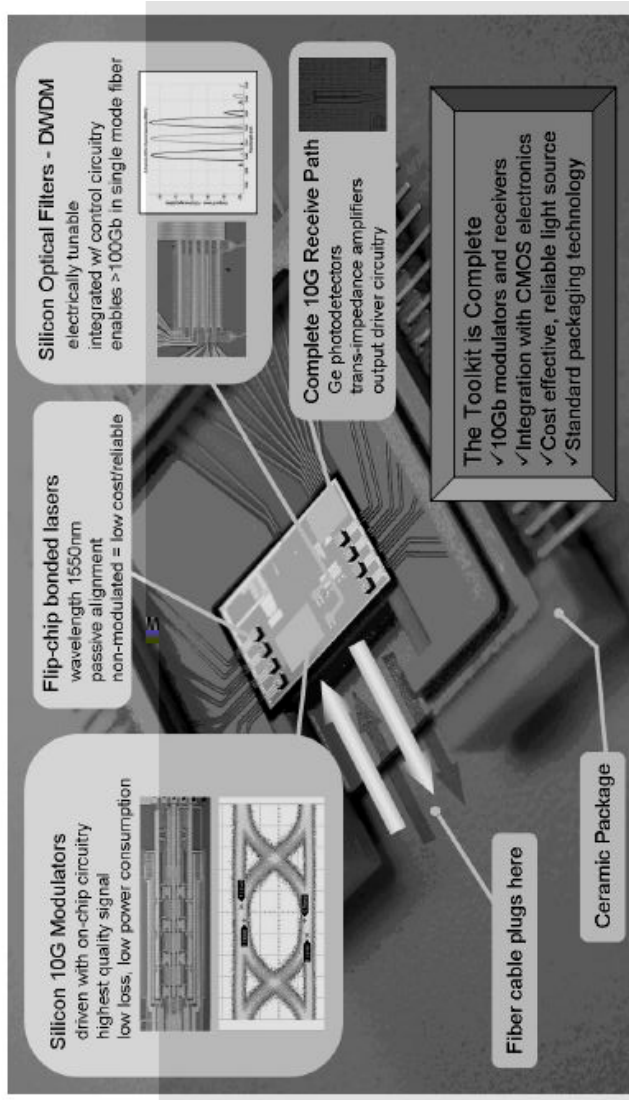


Figure 6. Overview of CMOS photonics technology.



Ref: C. Gunn, "CMOS photonics/spl trade/ - SOI learns a new trick", *Proceedings of the 2005 IEEE SOI Conference*, Oct. 3-5, 2005, pp.7-13.